Remarks

Reconsideration is respectfully requested in view of the above amendments and following remarks. Revisions of claims 1 and 19 are supported, for instance, in original claim 2. Accordingly, claim 2 has been canceled without prejudice or disclaimer. No new matter has been added. Claims 1, 3-6 and 19-21 are pending.

Claims 1-4, 6, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram et al. (U.S. Patent No. 6,051,878), in view of Bertin et al. (U.S. Patent No. 5,977,640), Panchou et al. (U.S. Patent No. 6,040,630) and Clayton (U.S. Patent No. 5,731,633). Applicant respectfully traverses this rejection, and respectfully requests reconsideration in view of the following comments.

Claims 1 and 20 are directed to semiconductor chip modules that include conductor units for connecting electrically the contact pads of the semiconductor chips and the circuit traces, where the conductor units include a plurality of conductive contact balls that are received in the holes in the dielectric tape members to establish electrical connection between the contact pads of the semiconductor chips and the circuit traces.

The present invention provides a semiconductor chip module structure that establishes good electrical connection between the module elements, particularly, the contact pads of the semiconductor chip and the circuit traces. Further, the contact balls that are received in the dielectric tape member help prevent the need for forming further structures on the substrate so that the semiconductor chip module can be manufactured in a fully automated manner resulting in lower production costs (page 18, lines 20-26), while still maintaining good electrical connection necessary, for instance in stacked modules.

Akram et al. is directed to a method of constructing stacked packages that include flip chips attached to substrates stacked atop one another by electric connections, which are column like structures. The electric connections achieve electric communication between the stacked substrates. Akram et al. includes substrates 116, 140 having electrical traces 136, 158 that provide electrical connection through the substrates. Semiconductor chips 162, 150 are mounted to top and bottom surfaces of the substrate through flip chip contacts 166. Bond pads 124, 144 are used for connecting the substrates 116, 140 together. Wirebonds 160 are used for connecting the semiconductor chip 150 to the substrate 140.

However, Akram et al. does not teach or suggest the features as required by claims 1 and 20. Particularly, Akram et al. does not teach or suggest conductor units for connecting electrically the contact pads of the semiconductor chips and the circuit traces, where the conductor units are a plurality of conductive contact balls that are received in the holes in the dielectric tape members to establish electrical connection between the contact pads of the semiconductor chips and the circuit traces in each module. In fact, Akram et al. teaches using wire bonding to connect the semiconductor chip to the substrate (Figure 1). To the extent that Akram et al mentions using a dielectric tape to connect a semiconductor chip to the substrate, which Applicant does not concede, the cited reference does not disclose a conductor unit structure used with the dielectric tape member, as required by claims 1 and 20. For at least these reasons, Akram et al. does not teach or suggest the features of claims 1 and 20.

Bertin et al., Panchou et al. and Clayton do no remedy the deficiencies of Akram et al. None of the cited references teach or suggest the conductor unit structure of conductive contact balls received in the holes of the dielectric tape member for connecting the semiconductor chip to the chip mounting member. Particularly, Panchou et al. discloses a thermoplastic attachment film 30 formed with vias 34 that accept conductive thermoplastic bumps 14 of the flip chip 11. The vias 34 also accept bond pads 38 that are formed by screen-printing on the substrate 31, where the thermoplastic attachment film 30 is positioned on the substrate 31 so that the vias 34 correspond with bumps 14 and the pads 38 to electrically connect the substrate with the flip chip 11.

However, the cited references including Panchou et al. do not disclose or suggest a conductor unit to connect the semiconductor chip with the chip mounting member having a structure of contact balls received in the dielectric tape member. As above, the present invention provides a structure where the semiconductor chip module structure maintains good electrical connection between the module elements, particularly, the contact pads of the semiconductor chip and the circuit traces of the chip mounting member. Further, the contact balls that are received in the dielectric tape member help prevent the need for forming further structures on the substrate so that the semiconductor chip module can be manufactured in a fully automated manner resulting in lower production costs (page 18, lines 20-26), while establishing good electrical connection necessary, for instance, in stacked modules. The cited references do not

discuss a structure as the claimed invention, or provide any solution to the problems that the present invention solves.

For at least the above reasons, the cited references either alone or in combination do not disclose the features of the present invention. Further, there is no suggestion in the cited references that would lead one of skill in the art to derive the features of the claimed invention or any of the advantages enjoyed by the claimed invention. It is respectfully submitted that claims 1 and 20 and dependent claims therefrom are patentable over the cited references.

Favorable consideration and withdrawal of the rejection are respectfully requested.

Claims 5 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram et al. (above) in view of Bertin et al. (above), Panchou et al. (above), Clayton (above), and further in view of Tanioka (U.S. Patent No. 5,784,264) and Londa (6,101,100). Applicant respectfully traverses this rejection, and respectfully requests reconsideration in view of the following comments.

Akram et al., Bertin et al., Panchou et al. and Clayton have been discussed above.

Claim 5 depends upon and further limits claim 1, the features of which have been discussed above. Claim 19 includes subject matter similar to claims 1 and 20, which have been discussed.

Tanioka and Londa do not further the teachings of the primary references in deriving the claimed invention. Tanioka is relied upon for disclosing epoxy resin materials for strengthening bonding between the semiconductor chip and the chip-mounting member. Londa is relied upon for disclosing solder balls aligned to the respective plated through holes so as to connect a modules to form a stacked configuration. However, Tanioka and Londa do not disclose the conductive unit structure to connect the semiconductor chip with the chip-mounting member, where the conductive units are contact balls received in the dielectric tape member, as required by claims 1 and 19. For at least these reasons, the cited references, either alone or in combination, do not teach the claimed invention and would not lead one of skill in the art to derive the features or the advantages enjoyed by the claimed invention. Accordingly, it is respectfully submitted that claims 5 and 19 are patentable over the cited references.

Favorable consideration and withdrawal of the rejection are respectfully requested.

With the above amendments and remarks, Applicant believes that the claims pending in this patent application are in a condition for allowance. Favorable consideration is respectfully requested. If any further questions arise, the Examiner is invited to contact Applicant's representative at the number listed below.

Respectfully submitted,

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